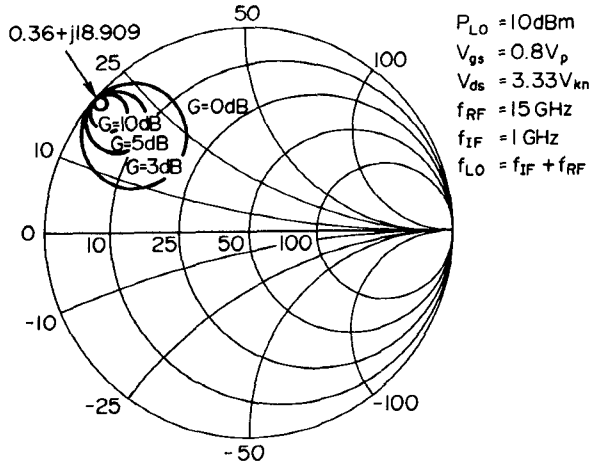

Fig. 4. Equal gain loci (RF source impedance) at RF frequency of 15 GHz. IF load impedance is fixed at $100+j100\ \Omega$.

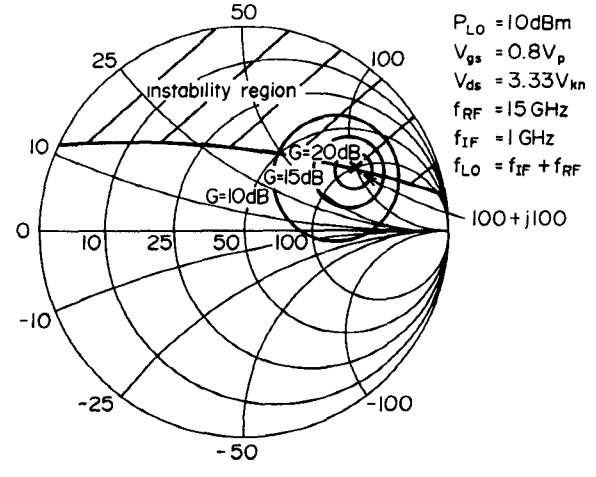

Fig. 5. Equal gain loci (IF load impedance) at RF frequency of 15 GHz. RF source impedance is fixed at $0.36+j18.91\ \Omega$.

gain loci of the IF load impedance under a fixed RF impedance of $0.36+j18.91\ \Omega$. At an IF output impedance of $100+j100\ \Omega$, the conversion gain is infinite, as expected. Fig. 5 shows that the tolerance of the IF load impedance is much wider than that of the RF source impedance. This means that the design accuracy of the RF input matching circuit mainly determines the maximum conversion gain.

IV. Conclusion

The MACG of a GaAs MESFET mixer has been estimated as a function of RF frequency under a fixed IF frequency of 1 GHz. The estimated conversion gain suggests that there are two unconditionally stable RF frequency regions. For the unconditionally stable RF frequency region, the optimum IF load impedance and the RF source impedance have been shown.

For the conditionally stable RF frequency region, stability circles and equal gain loci have been shown. The results suggest that instability can be avoided by increasing the RF source impedance slightly. The tolerance of the IF load impedance to obtain high gain is much wider than that of the RF source impedance. Thus, the maximum conversion gain of the actual mixer is mainly determined by the design accuracy of the RF source impedance.

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Projected Frequency Limits of GaAs MESFET's

J. Michael Golio and Janet R. J. Golio

Abstract—**Limits to the ultimate frequency performance which can be realized with GaAs MESFET's have been projected. These predictions are based on the reported performance of 137 devices fabricated between 1966 and 1988 and on first-order modeling. The predictions indicate that ultimate maximum frequency of oscillation values may approach 700 GHz while gain-bandwidth product values as high as 200 GHz may be realized.**

I. Introduction

The frequency limits of GaAs MESFET's have been extended each year since the device was first introduced in 1966 [1]. Most of the improvements have been realized by reducing the device dimensions (scaling). A study of scaling rules and limitations for GaAs MESFET's indicates that the physical properties of the device will require gate length dimensions to be greater than approximately 0.1 μm [2]. Although further reductions in gate length are technologically realizable, such devices will not exhibit improved frequency characteristics and will be useful only for a very limited number of applications.

Like the previous work, the present investigation confronts the scaling problem using an empirical–statistical approach in combination with some simple theoretical relationships. Gallium arsenide device manuscripts listed in the indexes of the IEEE Transactions on Microwave Theory and Techniques, the IEEE Transactions on Electron Devices, and the IEEE Electron Device Letters between 1966 and 1988 were considered for the investigation. During the early years of GaAs FET development, when few reports in the literature were available, other technical literature sources were also utilized. If the published report was not specifically stated to be for power or specialized applications, and information on at least two of the design details regarding gate length, epi-thickness, or doping density of the active channel was included, the device was used

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IEEE Log Number 9040569.

TABLE I
PUBLISHED REPORTS OF GaAs MESFET's FABRICATED OVER THE PAST 22 YEARS

1. Mead, *Proc. IEEE*, Feb. 1966
2. Hooper, *Proc. IEEE*, July 1967
3. Waldner, *Proc. IEEE*, Nov. 1969
4. Shapiro, *Proc. IEEE*, Nov. 1969
5. Statz, *Solid-State Electron.*, Dec. 1969
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13. Sitch, *Proc. IEEE*, Mar. 1973
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15. Baechtold, *Electron. Lett.*, Mar. 1973
16. Dean, IEEE MTT, Dec. 1973
17. Statz, IEEE TED, Sept. 1974
18. Liechti, IEEE MTT, May 1974
19. Anastassiou, IEEE MTT, Feb. 1974
20. Fair, IEEE TED, June 1974
21. Hunsperger, *Solid-State Electron.*, May 1975
22. Maeda, *Proc. IEEE*, Feb. 1975
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24. Barrera, IEEE TED, Nov. 1975
25. Liechti, IEEE MTT, June 1976
26. Baudet, IEEE MTT, June 1976
27. Pucel, IEEE MTT, June 1976
28. Hornbuckle, IEEE MTT, June 1976
29. Irie, IEEE MTT, June 1976
30. Ogawa, IEEE MTT, June 1976
31. Barnes, IEEE TED, Sept. 1976
32. Ohata, IEEE TED, Aug. 1977
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36. Abe, IEEE MTT, Mar. 1978
37. Sone, IEEE TED, Mar. 1978
38. D'Arso, IEEE TED, Oct. 1978
39. Takahashi, IEEE TED, Oct. 1978
40. Furutsuka, IEEE TED, June 1978
41. Suzuki, IEEE MTT, Dec. 1979
42. Fukui, IEEE MTT, July 1979
43. Hashizume, IEEE TED, Mar. 1979
44. Fukui, IEEE TED, July 1979
45. Mizuishi, IEEE TED, July 1979
46. Fukui, *Solid-State Electron.*, May 1979
47. deSantis, IEEE MTT, June 1980
48. Niclas, IEEE MTT, Mar. 1980
49. Ohata, IEEE TED, June 1980
50. Weinreb, IEEE MTT, Oct. 1980
51. Suyama, IEEE TED, June 1980
52. Imai, IEEE EDL, Mar. 1981
53. Levy, IEEE IEDM, Dec. 1981
54. Yokoyama, IEEE IEDM, Dec. 1981
55. Dekkers, IEEE TED, Sept. 1981
56. Tajima, IEEE TED, Feb. 1981
57. Oxley, IEEE IEDM, Dec. 1981
58. Beneking, IEEE TED, May 1982
59. Morcok, IEEE TED, Feb. 1982
60. Feng, IEEE EDL, Nov. 1982
61. Chye, IEEE EDL, Dec. 1982
62. Yokoyama, IEEE TED, Oct. 1982
63. Chen, IEEE TED, Oct. 1982
64. Feng, IEEE TED, Nov. 1983
65. Gupta, IEEE TED, Dec. 1983
66. Chao, IEEE EDL, Sept. 1983
67. Bandy, IEEE EDL, Feb. 1983
68. Imai, IEEE EDL, Apr. 1983
69. Chao, IEEE EDL, Apr. 1983
70. Kohn, IEEE EDL, Apr. 1983
71. deSalles, IEEE MTT, Oct. 1983
72. Gupta, IEEE MTT, Dec. 1983
73. Ohta, IEEE TED, Mar. 1984
74. Tomizawa, IEEE TED, Apr. 1984
75. Daembkes, IEEE TED, Aug. 1984
76. McNally, IEEE EDL, Apr. 1984
77. Feng, IEEE EDL, Mar. 1984
78. Feng, IEEE EDL, Jan. 1984
79. Mondal, IEEE MTT, Oct. 1984
80. Ayasli, IEEE MTT, Jan. 1984
81. Niclas, IEEE MTT, Mar. 1984
82. Chao, IEEE TED, June 1985
83. Ishida, IEEE TED, June 1985
84. Bastida, IEEE TED, Dec. 1985
85. Watkins, IEEE MTT-S, June 1985
86. Nair, IEEE TED, Sept. 1986
87. Fischer, IEEE TED, Feb. 1986
88. Gutmann, IEEE MTT-S, June 1986
89. Gupta, IEEE EDL, Oct. 1987
90. Zeghbroeck, IEEE EDL, May 1987
91. Hughes, IEEE TED, Apr. 1987
92. Mishra, IEEE/Cornell, 1987
93. Zhou, IEEE MTT-S, 1987
94. Hung, IEEE MTT, Dec. 1988
95. Bandla, IEEE MTT-S, 1988
96. Hegazi, IEEE MTT-S, 1988
97. Schindler, IEEE MMMCS, 1988
98. Gupta, IEEE MTT, Apr. 1988
99. Lan, IEEE MMMCS, 1988
100. Enoki, IEEE TED, June 1988
101. Banerjee, IEEE EDL, Jan. 1988
102. Pao, IEEE EDL, Mar. 1988
103. Harder, IEEE EDL, Apr. 1988
104. Lo, IEEE EDL, Aug. 1988
105. Onodera, IEEE EDL, Aug. 1988
106. Tehrani, IEEE TED, May 1988
107. Bernstein, IEEE TED, July 1988
108. D'Avanzo, IEEE GaAsIC-S, 1988
109. Chang, IEEE TED, Oct. 1988

Key:
TED: TRANSACTIONS ON ELECTRON DEVICES
MTT: TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES
EDL: ELECTRON DEVICE LETTERS
IEDM: *International Electron Devices Meeting Digest*
MTT-S: *International Microwave Symposium Digest*
IEEE/CORNELL: *Proceedings of the IEEE/Cornell Conference on Advanced Concepts in High-Speed Semiconductor Devices and Circuits*
MMMCS: *IEEE Microwave and Millimeter-Wave Monolithic Circuits Symposium Digest*
GaAsIC-S: *Gallium Arsenide Integrated Circuits Symposium Digest*

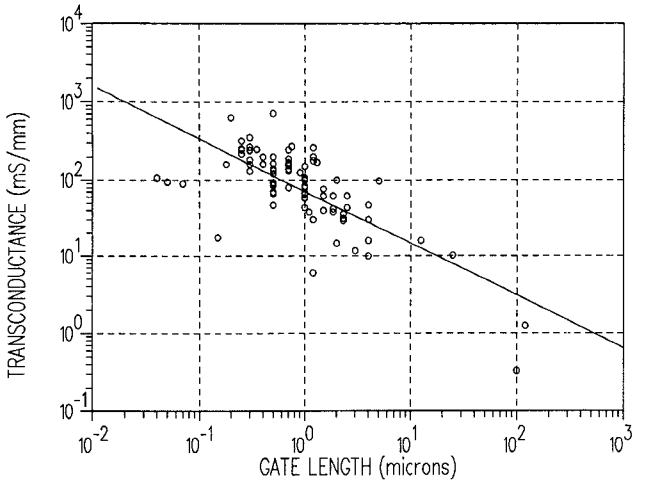

Fig. 1. Reported transconductance per unit gate width as a function of reported gate length. The devices used to produce the figure are from the reports of Table I.

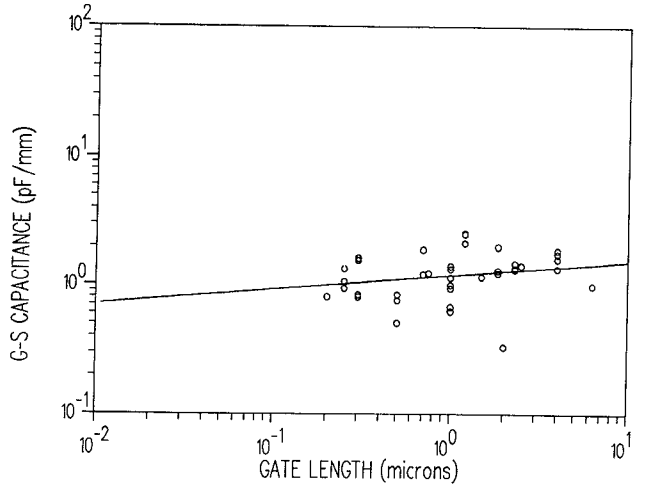

Fig. 2. Reported gate–source capacitance per unit gate width as a function of reported gate length.

in the data base for the current analysis. The 109 publications used to compile the frequency performance data are listed in Table I.

From the data, relationships between device gate length and performance figures of merit are discovered. The relationships are used to estimate frequency limits of GaAs MESFET's.

II. Transconductance and Gate–Source Capacitance

Figs. 1 and 2 present reported transconductance and gate–source capacitance as a function of gate length for the reported devices. The curves presented in these figures are obtained by computing the least-squares fit straight line to the data.

As expected from device theory, the reported transconductance increases with decreasing gate length. The straight line fit for transconductance reaches a value of 338 mS per mm of gate width for a gate length dimension of 0.1 μm. The g_m value of 338 mS/mm laying on the line is obtained using all devices for which a g_m value is presented. Such a value underestimates the ultimate transconductance achievable since it makes use of data taken on devices which were not optimum as well as those which approach optimum. The transconductance data from only the best devices can be used to argue for g_m values exceeding 1000 mS/mm at a gate length dimension of 0.1 μm.

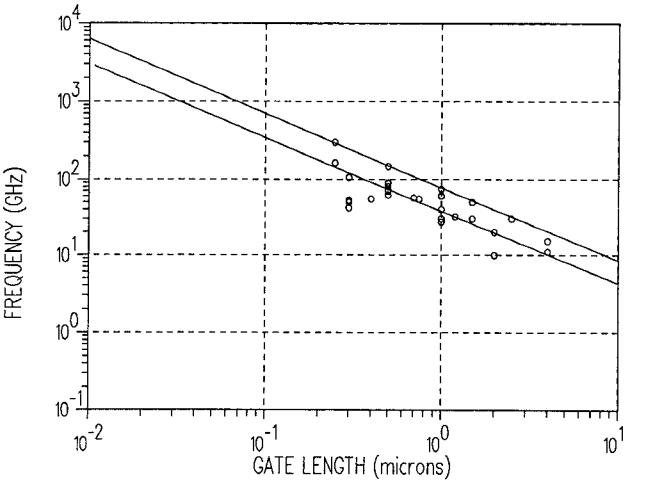

Fig. 3. Reported or calculated maximum frequency of oscillation, f_{max}, as a function of reported gate length.

Reported transconductance values consist of a combination of dc and RF values. Although measured RF transconductance is typically 10% to 20% lower than measured dc values, no attempt to distinguish between these has been made in this study. This accounts for some of the observed scatter in the data.

In contrast to the transconductance data, the reported gate–source capacitance presented in Fig. 2 exhibits very little gate length dependence. For proper scaling, the reduction of device gate length (which reduces C_{gs}) requires increases in doping density (which increases C_{gs}). These two scaling procedures tend to negate each other, and the reported gate–source capacitance has remained at approximately 1 pF/mm for most of the reported devices.

III. Maximum Frequency of Oscillation

Fig. 3 presents the reported maximum frequency of oscillation, f_{max}. Devices described in the reports of Table I which do not present f_{max} values are still used to accumulate these data if enough information is presented regarding an equivalent circuit of the device to compute an f_{max} value. The expression used to determine the maximum frequency of oscillation of the device is taken to be [3]

$$f_{max} = \frac{f_T}{2}\left[\frac{R_{ds}}{R_g}\right]^{1/2} \tag{1}$$

where R_{ds} is the device output resistance, R_g is the parasitic gate resistance, and f_T is the gain–bandwidth product for the device. The least-squares fit line to the data (lower curve in Fig. 3) predicts an f_{max} value of 341 GHz for a gate length of 0.1 μm. The equation for the f_{max} least-squares fit is given by

$$f_{max} = 38.05L^{-0.953}. \tag{2}$$

Using only the highest reported values for f_{max} to extrapolate ultimate limits, a frequency of approximately 700 GHz is associated with a 0.1 μm gate length device (upper curve in Fig. 3).

IV. Gain–Bandwidth Product

The reported gain–bandwidth product, f_T, is presented in Fig. 4. If f_T values are not published but sufficient equivalent circuit information is provided, values for f_T are calculated. For

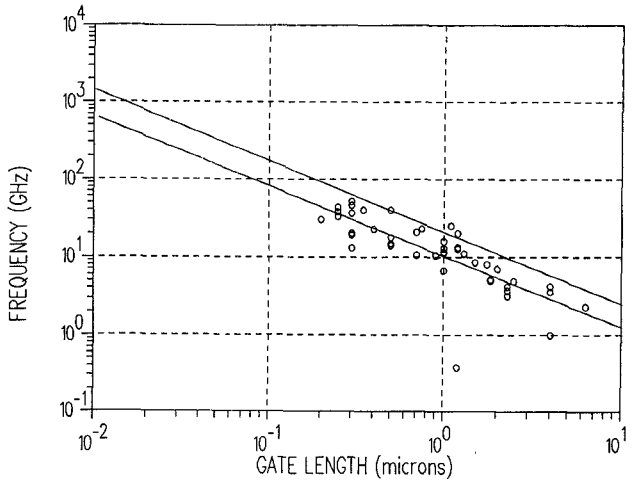

Fig. 4. Reported or calculated gain–bandwidth product, f_T, as a function of reported gate length.

convenience, the first-order expression

$$f_T = \frac{g_m}{2\pi C_{gs}} \tag{3}$$

is used for these calculations. Expression (3) will tend to overestimate the gain–bandwidth product of a device with small gate-length dimensions. Many of the published values of f_T have been determined from more accurate expressions or from extrapolation of the $|h_{21}|$ versus frequency curve to unity. Some of the observed scatter in the data of Fig. 4 is due to the differences in the methods used to compute f_T.

In Fig. 4 the f_T values published for devices with gate length dimensions of 0.25 μm or less lie on or below the least-squares fit line. Explanations which can be offered for this less than outstanding performance include: 1) physical limitations are already being reached and FET scaling cannot continue to advance device performance, and/or 2) fabrication technology required to realize such devices has not yet matured.

Based on earlier examination of the first explanation [2], it is probable that higher f_T values for these small gate length devices will be achieved when fabrication procedures to deal with special problems of short gate devices have been developed or improved. The ideal scaling suggested in [2] requires that a 0.25 μm gate length device be doped to a level as high as 1.1×10^{18} cm^{-3} and have an epi-layer thickness of less than 0.08 μm. The status of processing technology today makes it difficult to achieve superior quality layers with these specifications. Among the problems unique or more critical to the small gate length devices are transient velocity phenomena (e.g. velocity overshoot), channel–substrate interface effects (e.g. carrier confinement), and the effects of surface states. As doping density is increased, shorter dimensions are required for velocity overshoot to be observed. For the combination of channel dimensions/doping densities required for optimum scaling [2], transient velocity phenomena do not constitute a dominant factor. Velocity overshoot, however, may have a second-order effect on both the f_T and the f_{max} performance. Solving problems regarding the channel–substrate interface and surface states may require that more complex processing techniques be developed. Reduction of undesirable effects at the channel–substrate interface, for example, might involve fabrication of the active channel on wide-band-gap or superlattice layers. Likewise, solution of surface state issues may require fabrication of buried channel structures [5].

TABLE II
COMPARISON BETWEEN THE PROJECTED DEVICE CHARACTERISTICS PREDICTED BY EQUATION (4) AND THOSE FORMULATED BY FUKUI [4]

Gate Length (μm)	f_T from Eq. (4) (GHz)	f_T after Fukui [4] (GHz)
0.05	153	188
0.1	82	94
0.5	19	19
1.0	10.2	9.4
5.0	2.4	1.9

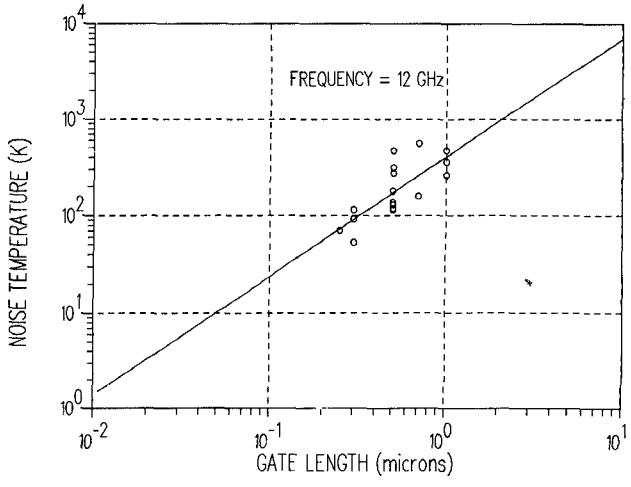

Fig. 5. Reported minimum noise temperature measured at 12 GHz as a function of reported gate length.

A least-squares fit to the data of Fig. 4 is expressed by

$$f_T = 10.20L^{-0.905}. \tag{4}$$

When evaluated for $L = 0.1$ μm, (4) predicts an f_T value of 82 GHz. Use of only the highest f_T data to extrapolate frequency limits of a 0.1 μm device (upper curve of Fig. 4) indicates that an f_T value of nearly 200 GHz may be achievable.

Equation (4) can be compared directly with the expression derived by Fukui [4] for gain–bandwidth product as a function of gate length. The Fukui expression is

$$f_T = \frac{9.4}{L}. \tag{5}$$

Table II presents this comparison. The two expressions are seen to be in remarkable agreement except at very small gate length dimensions.

V. Noise Figure

As with other performance parameters, it is possible to analyze minimum noise characteristics using the data presented in the technical literature. The minimum noise figure of a device, however, is not always measured at the same frequency. Thus, fewer data are available at any one frequency than for other performance figures of merit. As expected, the frequencies at which the minimum noise figure is presented in the literature increase with decreasing gate lengths. The projections of device noise presented here should therefore be viewed with some caution.

Fig. 5 presents the measured minimum noise temperature at 12 GHz. The least-squares fit to the data predicts that a noise temperature of 23.81° will be realizable for 0.1 μm gate length

devices. This corresponds to a minimum noise figure of 0.34 dB. The minimum noise figure at 18 GHz for a 0.1 μm device, projected in an identical manner, is 1.2 dB.

VI. Conclusions

Reported device performance from the technical literature published from 1966 to 1988 was analyzed to predict ultimate frequency limits of GaAs MESFET's. The data indicate that gain–bandwidth products in the range of 200 GHz and maximum frequencies of oscillation of the order of 700 GHz may be achievable with GaAs MESFET structures. Previous work [2] indicates that if progress continues at the present rate, such performance will be achieved by the year 1997. Achieving the projected performance will almost certainly require advances in current process technology. Although 0.1 μm devices have already been fabricated, optimally scaled devices with superior material quality and an absence of surface and channel–interface states have not been achieved. Further advances in frequency performance will be possible with other solid-state transistors such as InP FET's or HEMT's, which were not considered to form the data base for this study.

The data presented can also be used as a standard upon which to judge device scaling efforts. If appropriate device scaling has been achieved, GaAs FET figures of merit should fall on or above the curves presented here.

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A Method of Tolerance Enhancement for Filters and Amplifier Matching Networks

A. N. Riddle and R. J. Trew

Abstract—**A new filter prototype for increasing the tolerance of passive networks to load variations is presented. A method based on the way in which a network's reflection coefficient changes in response to component and load reactance variations is used to develop the filter polynomial. This new filter polynomial has greater tolerance to load reactance variations, component variations, and finite element Q than Butterworth, Chebyshev, or elliptic structures. Examples using this new filter for tolerance enhancement of filters and matching structures are presented.**

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IEEE Log Number 9040568.

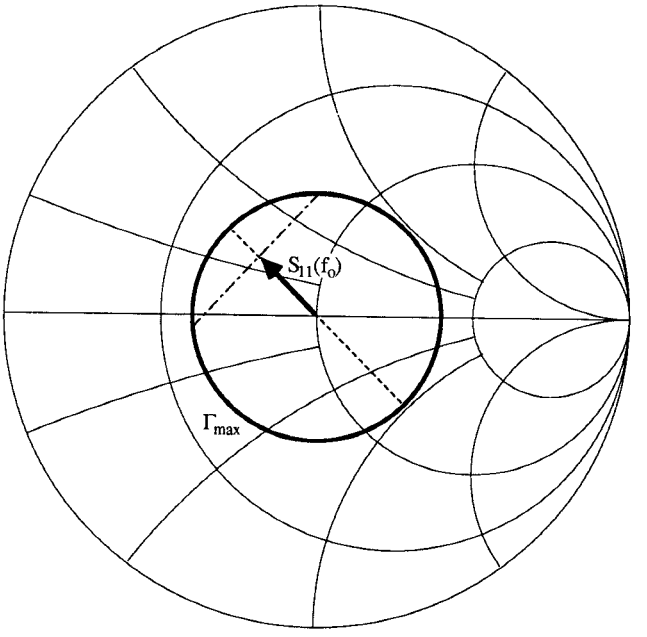

Fig. 1. A Smith chart containing the maximum tolerable reflection, Γ_{max}, and the input reflection coefficient at f_0, $S_{11}(f_0)$. The dashed radial line represents the direction of minimum absolute variation in $S_{11}(f_0)$. The alternating line perpendicular to the $S_{11}(f_0)$ vector represents the direction of maximum absolute tolerance since the distance between $S_{11}(f_0)$ and the $S_{11\,max}$ circle is maximized.

I. Introduction

To date little work has been reported on appropriate design procedures for high-tolerance matching networks. A new method for designing suitable matching networks is presented in this paper. In particular, a solution to the approximation problem for deriving filters with greater tolerances to load parasitics, loss, and element tolerances is presented. The filter polynomial represented in this paper is intended to be used with synthesis procedures discussed elsewhere [1], [2]. Only lumped element prototypes are considered so that the effects of the filtering function, rather than a particular realization method, may be studied.

The first detailed consideration of ideal responses for matching filters was presented by Fano [3]. Although Fano demonstrated that a low-ripple Chebyshev response approximating a constant mismatch was superior to a large-ripple Chebyshev response with the same peak mismatch, he did not explore filter responses other than Butterworth, Chebyshev, and elliptic types.

The filter polynomial developed in this paper was designed to maximize the filter's tolerance to load reactance variations. Load reactance variations typically would be changes in FET input capacity or bond wire inductance. Since the sensitivity to reactance variations is reduced, both lead inductance and device capacitance variations have less effect on the amplifier response when this filter prototype is used to design the matching network.

This new filter response was derived from geometrical considerations in the reflection coefficient plane (Fig. 1). Amplifiers and filters are specified not to exceed a certain reflection coefficient. Let this specification be the Γ_{max} circle shown in Fig. 1. Tolerant networks allow greater variations in circuit components before the response exceeds this Γ_{max} circle. The $S_{11}(f_0)$ vector shown in Fig. 1 represents a circuit's response at one

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